ABSTRACT OF THE DISCLOSURE

A channel erase flash memory including a redundancy word line group constituted of a plurality of redundancy word lines separately from a normal memory space of a memory cell array, and including a function of replacing the normal word line group including a defective memory cell with the redundancy word line group. In the memory, at the time of an erase operation, a first voltage is applied to a well region in which the memory cell array is formed, a second voltage of 0 V or less is applied to a normal word line, and a third voltage is applied to all the word lines included in the normal word line group including the defective memory cell or the redundancy word line group. A potential difference between the first and third voltages is set to be smaller than that between the first and second voltages.